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**Patrik Algotsson et al.** § Group Art Unit:  
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Title: **A Method to Provide a Triple Well**  
in an Epitaxially Based CMOS or  
BiCMOS Process § Client Ref.: **P 04-120/FA/PIA**  
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**SUBMISSION OF PRIORITY DOCUMENT**

Dear Sir:

We enclose herewith a certified copy of Swedish patent application 0300924-8 filed March 28, 2003 which is the priority document for the above-referenced patent application.

BAKER BOTTS L.L.P. (023640)

Date: March 26, 2004

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# PRV

PATENT- OCH REGISTRERINGSVERKET  
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This is to certify that the annexed is a true copy of the documents as originally filed with the Patent- and Registration Office in connection with the following patent application.

(71) Sökande            *Infineon Technologies Wireless Solutions Sweden AB*  
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Stockholm, 2004-03-12

För Patent- och registreringsverket  
For the Patent- and Registration Office

*Hjördis Segerlund*  
Hjördis Segerlund

Avgift  
Fee        170:-

PATENT DEPARTMENT

A method to provide a triple well in an epitaxially-based  
CMOS or BiCMOS process

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2003-03-28

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**Technical field of the invention**

The present invention relates to a method to provide a triple well in an epitaxially based CMOS or BiCMOS process.

**Background of the invention**

5 In a main stream CMOS or BiCMOS process a PWELL/pwell in an NMOS can be implanted in a P/p-type substrate and thereby the biasing of the pwell is common for all the NMOS transistors on a chip. In order to prevent a global biasing, a TRIPLE WELL/triple well option can be used. The use of a  
10 triple well is earlier known and a method to provide a triple well has been earlier published, see e.g. US Patent No 6.388.295 and Japanese Patent No. 11026601.

15 The use of a triple well firstly provides an opportunity to have a separate biasing on each NMOS transistor and hence adjust a threshold voltage individually. For an analogue RF and perhaps most desirably for mixed signals circuits the use of a triple well also isolates the NMOS transistors and suppresses noise couplings. There are several benefits, which can be achieved by using a triple well concept. In an  
20 integrated circuit a global biasing for a group of transistors can be of advantage.

**Summary of the invention**

25 The present invention relates to a new method to provide a deep NWELL/nwell such as a triple well. The conventional process flow using triple well has an implanted phosphorous doping deep into the silicon, fabricated by using a high energy implant. This invention instead suggests the use of arsenic doping implanted prior to the deposition of the  
30 epitaxial layer. Arsenic is preferable since it diffuses slower than phosphorous and has a better lattice match. Said arsenic is implanted deep into the silicon to minimise its

*Huvudfakten Kesson*

influence on the transistor parameters. The depth of a subsequent pwell implant after an epitaxial deposition of the NMOS transistor determines the depth of the triple well implant. The method is preferably intended for a Shallow Trench Isolated (STI) process. The depth of the STI must not reach this arsenic implanted triple well. This means that some additional N-type doping must be introduced to cut the path beneath the STI. This can be made using an additional N implant in sequence with the triple well implant prior to an/the epitaxial deposition. The standard nwell implant of the PMOS transistor may also be used to cut this path. This nwell implant is performed after the STI etch and fill. The energy is chosen in such a way that the N-type doping will reach the area underneath the STI and together with the deep nwell form a good isolation of the PMOS transistor.

The introduction of said deep N-implant prior to the epitaxial deposition essentially constitutes the substance of the first claim of the invention. The use of arsenic in this kind of application constitutes the substance of the second claim of the invention.

This process sequence may easily be added to a standard CMOS/BiCMOS process flow. By using this concept it will be possible to have a group of NMOS transistors in one and the same island, isolated from its surrounding. This invention even states that a group of NMOS transistors, which will have the same biasing should be surrounded by the standard NWELL implant or an additional N type implant prior to the epitaxial deposition, which essentially constitutes the substance of the third claim of the invention.

An adding of an additional boron doping added beneath the STI essentially constitutes the substance of the fourth claim of the invention. Depending on type or process, the resistivity p-type path under the STI could be high, which requires short distance between pwell contacts. To be able

2003-03-28

3

Huvudforsen Kassan

to increase this distance an additional p-type implant can be introduced prior to the epitaxial deposition in the same way as the deep well/DEEP NWELL implant. This implant must be optimised in such way that it does not cut through the 5 triple well/TRIPLE WELL implant and establish a conductive path to the substrate. The pwell of the NMOS transistor may be designed in such a way that it reaches deeper than the STI depth and thereby decrease the resistance of the current path underneath the STI.

10 Brief description of the drawings

Figure 1 is a sectional view of a p-type substrate.

Figure 2 is a sectional view of the p-type substrate with an implanted triple well according to the invention.

15 Figure 3 is a sectional view of the p-type substrate with the implanted triple well according to the invention, where an implantation of n-type dopant is shown.

Figure 4 is a sectional view of the p-type substrate with the implanted triple well according to the invention, where an implantation of a p-type dopant is shown.

20 Figure 5 is a sectional view of the p-type substrate with the implanted triple well according to the invention, where an isolation between achieved different islands is shown.

Figure 6 is a sectional view of the p-type substrate with the implanted triple well according to the invention with 25 three NMOS transistors.

Preferred embodiments of the invention

In order to understand the present invention a particular example will be described. Details known by persons skilled in the art are omitted. The following description is a 30 sequence of process steps and can be dropped into a main

stream CMOS or BiCMOS process as a separate module. No details are given about the flow before or after those process steps. The alignment marks are also assumed to be made in an earlier step and can be used in the described sequence.

In figure 1 there is shown a sectional view of a p-substrate 1. The doping level for the substrate is chosen depending on the application for the circuit. The concept will not be affected by the choice of resistivity as long it is high ohmic.

On this starting material a sequence of three implantations prior to an epitaxial deposition will follow. A first mask 2 is applied to achieve a triple well 3 in preferable areas. The mask 2 has openings only in areas right above those areas. Using this patterned resist 2 as a mask an ion implant 4 of arsenic is followed. This implant 4 having a suggested doping dose of  $2 \times 10^{13}$  cm<sup>-2</sup>, energy of 480 keV and a tilt angle of 0 degree penetrate deep into the substrate. In figure 2 the step is shown of this implant and the achieved triple well region 3.

A next mask step 5 is made to mask an additional n-type implant 6 that will surround the device or group of devices in a same island. This implant must be made in such a way that no p-type will remain under a STI 12a in implanted areas. It must also connect to the triple well to make sure that no p-type region will separate this implant from the triple well. In figure 3 the implantation of this n-type dopant is shown.

A last doping 8 is aimed to end up under the STI 12b that will be performed later in the process flow. It will have a separate patterned resist mask 9. The dose and the energy of this implant was chosen so it reaches the triple well 3. It should be as high as possible but still not cut the triple

2003-03-28

Huvudfaxen Kassan

well 3. Even lateral diffusion that might have impact on design rules must be taken under consideration when the dose and energy are to be determined. When the design rules are set the implantation should be optimised in such a way that 5 the resistivity for current path under the STI should be minimised. In figure 4 the implantation of this p-type doping is shown.

This description gives those three implants a particular sequence. But any permutation in the order of the 10 implantation can be made and still the wanted structure can be achieved.

After those three masked implantations an epitaxial growth will be performed. A masked etch into the silicon will follow into this epitaxial layer. Obtained trenches will be 15 filled by a dielectric material, as High Density Plasma oxide (HDP), and then planarized by chemical and/or mechanical polishing CMP. Those boxes, STI 12, will provide the isolation between the devices in the process as shown in figure 5. So far no absolute number of depth and thickness 20 has been mentioned. The reason is that this concept will work in a wide range for those numbers. But the following condition is required to make the concept to work. The epitaxial thickness, STI depth and the depth of said three implantations must be related to each other as follow. The 25 STI should not reach the triple well. The p-type should not be implanted in the area where the n-type will be implanted. The surrounding n-type must reach the triple well and cut all p-type under the STI in implanted areas. The triple well must be deep enough to not have any major impact on the behaviour of the transistor.

The numbers of mask step are a figure of the complexity of the technology. In this sequence three additional layer are included to the basic process flow. To reduce this to only one extra mask, pwell implantations can be used instead of 8

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and nwell or buried collector can be used instead of .6 and this will reduce the processing cost.

In this achieved structure a conventional NMOS devise can be created by conventional main stream CMOS or BICMOS flow. In 5 figure 6 cross sections of three NMOS transistors are shown. Terminals to pwell 6 and triple well 3 are not visible in the view. Drain 14, source 15 and gate 13 can be seen in the figure. If a single device will be biased separately the additional p-type implant is not necessary. In that case the 10 surrounding STI 12a is the same STI as the STI 12b that isolate the device. Which means that the additional n-type implant will be under the same STI as the STI isolating the device. In the case when more than one device will be made and the same island this additional n-type will only be 15 under the surrounding STI. The p-type will be under the STI captured by this surrounding STI and n-type implant.



7

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Claims

2003-03-28

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1. A method to provide a triple well in an epitaxially based CMOS or BiCMOS process, characterised by implanting the triple well prior to the epitaxial deposition.
- 5 2. A method according to claim 1, characterised by using arsenic when implanting the triple well, wherein a slow diffusion will occur.
3. A method according to claim 2, characterised by adding at least one NMOS device in an achieved structure.
- 10 4. A method according to claim 2 or 3, characterised by implanting Boron prior to the epitaxial deposition.
5. A method according to claim 4, characterized by adding more than one NMOS device in an achieved structure.

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2003-03-28

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## 1 P-substrate

Fig 1

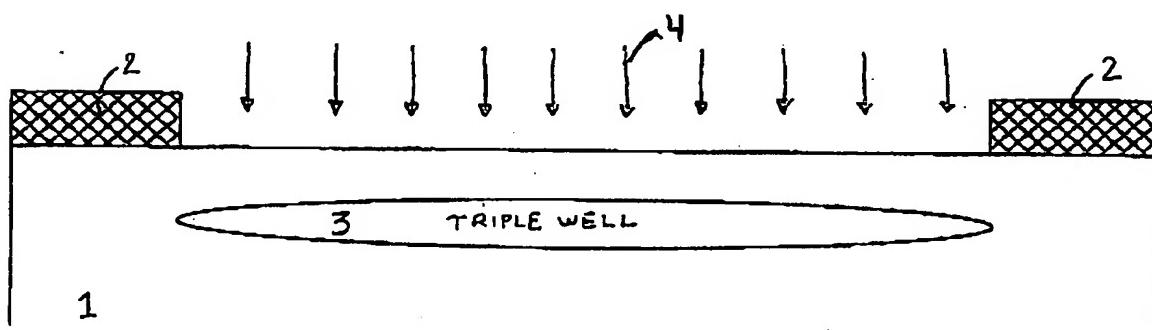


Fig 2

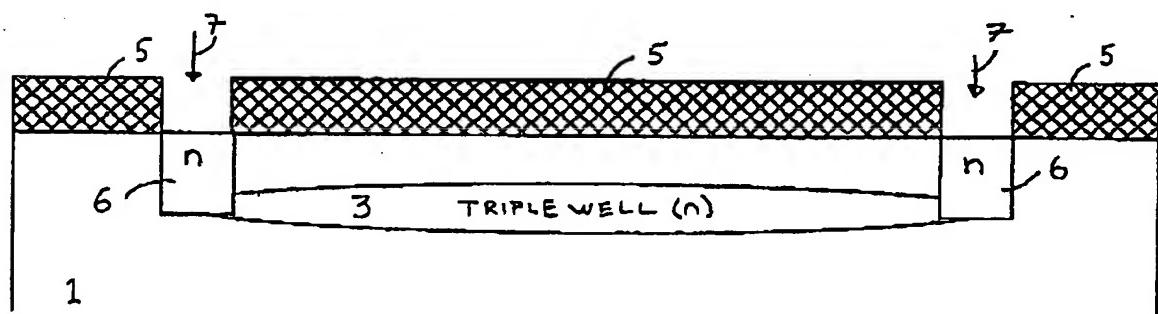


Fig 3

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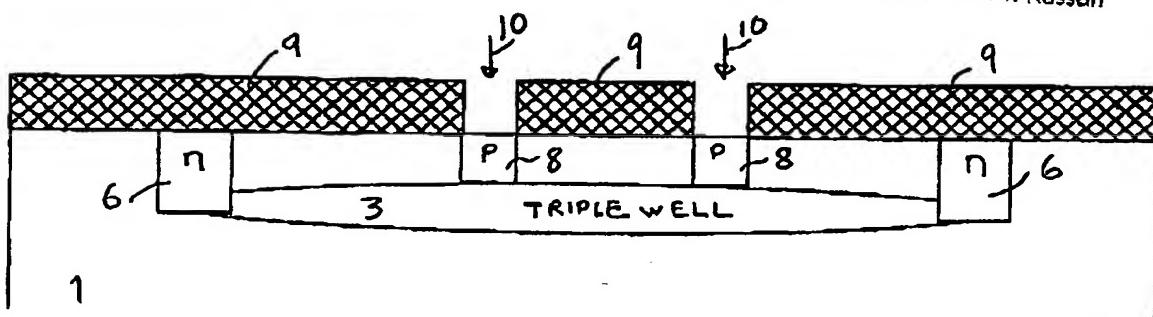


Fig 4

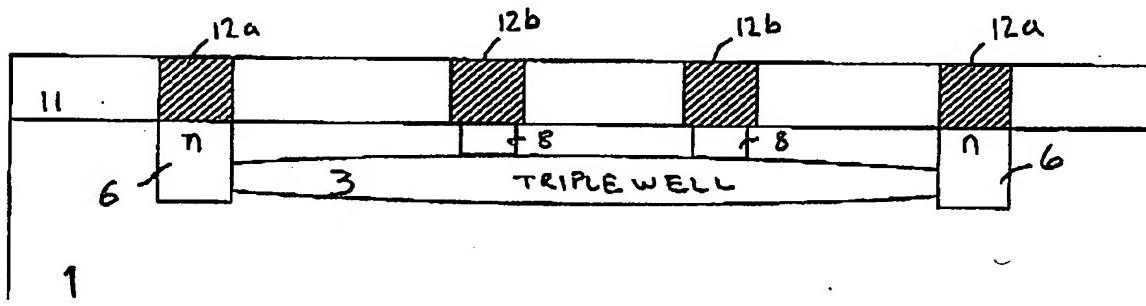


Fig 5

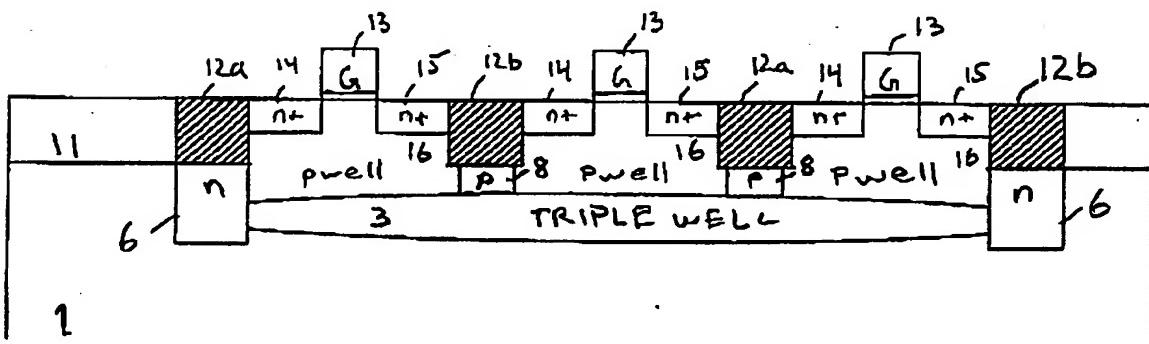


Fig 6